A Novel approach towards performance analysis Of Vedic multiplier using FPGA’s

Shivakumar M V
M.Tech Dept of ECE
Reva Institute of Technology
Bangalore, Karnataka
India

Mrs. Anitha Kumari
Assistant Professor, M.Tech
Dept of ECE, Reva Institute of Technology
Bangalore, Karnataka
India

Abstract—This Paper proposes the implementation of multiplier using ancient Indian vedic mathematics (Urdhva-tiryagbhyam) that has been modified to improve performance of high speed mathematics, it shows the modified architecture for a 16*16 Vedic multiplier module using Urdhva-tiryagbhyam technique. The design implementation is described in both at gate level and high level RTL code using Verilog Hardware Discription Language. The design is Simulated and Implemented using Xilinx ISE 11.1 Simulator, Xilinx Family: Vertex 2P, Device: XC5VLX30, Speed Grade: -7 and Xilinx Family: Spartan 3AN, Device: XC3S50A, Speed grade: -5

Keywords— Multiplier, Spartan 3AN, Virtex, Urdhva-tiryagbhyam

I. INTRODUCTION

Vedic mathematics is the name given to the ancient Indian system of mathematics that was recovered in early twentieth century. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Triyakbayam (Vertically and Cross wise) Sutra is presented, This Sutra was traditionally used for the multiplication of two decimal numbers relatively in less time. In this paper, after gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware, the conventional mathematical algorithm can be simplified and even optimized by the use of Vedic mathematics, the Vedic algorithms can be applied to arithmetic, trigonometry, plain and spherical geometry, calculus.

The power of Vedic mathematics not only confined to its simplicity, regularity, but also it is logical. Its high degree of eminence is attributed to the aforementioned facts. It is these phenomenal characteristics, which made Vedic mathematics, become so popular and thus it has become one of the leading topics of research not only in India but abroad as well, multipliers based on Vedic multiplication are one of the fast and low power multipliers. Minimizing the power consumption for digital system involves optimization at all levels of the design and in Vedic multiplication this is achieved due to less step to solve multiplication than the traditional multiplication.

The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

We have developed new Vedic multiplier structure using Urdhav-tiryagbhyam sutra with
reduced delay and power consumption compared to conventional multipliers and performance of Vedic multiplier analyzed by Vertex and Spartan 3AN FPGA’s and we found computation delay of Vedic multiplier is less in Vertex when compared with Spartan 3AN.

II. VEDIC ALGORITHM

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed, Vedic multiplier can be used as the building blocks in the design of Arithmetic & Logic Unit (ALU), Multiply & Accumulate (MAC), DFT, FFT, DST, DSCT etc. and the number of garbage outputs, delay and power dissipation of Vedic multiplier can be reduced further by improvising the design. Delay and power dissipation can be further optimized by optimizing the layout of the circuit.

Vedic multiplier has reduced delay compared to the circuits using basic gates. Therefore Vedic multiplier can be implemented in the processors, digital signal processing units for faster computation.
III. MULTIPLIER ARCHITECTURE

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig.

![Figure 3] Implementation of 2X2 Vedic multiplier

Multiplication of two bit binary numbers.

<table>
<thead>
<tr>
<th>Step 1</th>
<th>Step 2</th>
<th>Step 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0</td>
<td>1 0</td>
<td>1 0</td>
</tr>
<tr>
<td>1 0</td>
<td>1 0</td>
<td>1 0</td>
</tr>
</tbody>
</table>

![Figure 3] Multiplication of two bit binary number

The RTL view of 2X2 multiplier as shown in fig.

The 4X4 Vedic multiplier module is implemented using two 2X2 multiplier as shown in fig, same way 8X8 can be implemented using two 4X4 module and 16X16 can be implemented using two 8X8 module,This in turn reduces delay, which is the primary motivation behind this work.

![Figure 4] RTL view of 2X2 Vedic multiplier.

![Figure 5] Implementation of 4X4 Vedic multiplier.

IV. PROPOSED BLOCK DIAGRAM

![Figure 6] Proposed block diagram.
Figure shows proposed block diagram to design and implementation of Vedic multiplier and analyze the performance with different FPGA processors are Vertex 2P and Spartan 3AN and we found that worst case delay of Vedic multiplier using Vertex 2P is less when compare to worst case delay of Vedic multiplier using Spartan 3AN, result shows that performance of Vedic multiplier more efficient in Vertex processor when compared with Spartan processor, this design can be implemented in Modern Broadband communication where large number of complex.

This design can be further implemented and tested to optimize delay of Vedic multiplier with dedicated high end processor.

V. RESULT & DISCUSSION

Figure shows result of 2X2 Vedic multiplier.

![Figure (7) Result snap of 2X2 Vedic multiplier.](image)

Figure shows result of 4X4 Vedic multiplier.

![Figure (8) Result snap of 4X4 Vedic multiplier.](image)

Figure shows result of 8X8 Vedic multiplier.

![Figure (9) Result snap of 8X8 Vedic multiplier. Figure shows result of 16X16 Vedic multiplier.](image)

The Proposed 16X16 Vedic multiplier using Urdhva Tiryakbhyam Sutra found to be better than other conventional multiplier in terms of Delay and Speed, and the performance of Vedic multiplier found better with Vertex 2P processor when compared with Spartan 3AN.

a. Comparison of Simulation and Synthesis Report

<table>
<thead>
<tr>
<th>Device</th>
<th>Delay</th>
<th>No of Slices</th>
<th>LUT’s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertex 2P</td>
<td>16.417ns</td>
<td>13696</td>
<td>27392</td>
</tr>
<tr>
<td>Spartan 3AN</td>
<td>21.647ns</td>
<td>960</td>
<td>1920</td>
</tr>
</tbody>
</table>

The Comparison of Simulation and Synthesis Report On Vedic multiplier shows that the time required to produce the output is less on Vertex 2P Processor over Spartan 3AN Processor, further comparison of synthesis report as follows.
VI. CONCLUSION
This paper presents a highly efficient method of 16X16 multiplications – “Urdhva Tiryakbhyam Sutra” based on Vedic mathematics, This Vedic multiplier architecture shows speed improvements over conventional multiplier, In this project we have been successful in verifying the 16X16 Vedic multiplier algorithm of Urdhva Triyakbhyam sutra over basic gates and analyzing performance on FPGA’s, From the simulation and analysis results shows that worst case delay of 16 bit Vedic multiplier using Vertex 2P is 16.417ns which is less when compared with Spartan 3AN delay of 21.647ns.Future work includes the integration of the divider block, multiply and accumulate (MAC) unit, thereby making it into a Vedic Arithmetic and Logical unit (ALU) for dedicated processor, We implemented and tested design using Vertex and Spartan processor, this design can be further optimized and tested with dedicated high end processors.

VII. REFERENCES


[8].Shamim Akhter.“VHDL implementation of Fast NXN Multiplier Based on Vedic Mathematics”, Jaypee Institute of Information Technology University, Noida, 2013 07 UP, INDIA, 2007 IEEE